REMARKS

This amendment is submitted as a full and complete response to the Office Action dated September 26, 2007. Reconsideration and allowance of the claims are requested. The independent claims have been amended in each instance to more distinctly claim the subject matter that the Applicants regard as the invention. Claims 16, 19, and 20 are cancelled. An explanation of each amendment appears below.

Claims 1, 3-4, 9-10, and 20

Claims 1, 3-6, 9-10, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Zolnowsky* (U.S. Patent No. 5,826,081) and *Jones* (U.S. Patent No. 5,812,844). These rejections are respectfully traversed.

Applicant is amending independent claims 1 and 9 to include the limitations of (i) simultaneously rearranging threads in a single queue and ordering all requests from the hardware devices in the single queue. The single queue represents the order in which all threads will be serviced for all of the hardware devices. As described in paragraph [0044] of the present application, the scheduler "rearranges various threads in the queue such that threads that require faster service based on latency will be processed ahead of other threads that can wait a bit longer." As stated in the paragraph [0004] of the background section of the present application, some prior art systems use two queues, where one queue is dedicated to high priority processes and another queue is dedicated to address low priority processes in order to meet real-time processing constraints. In the invention, single queue orders threads corresponding to requests from all of the hardware devices. Additionally, the threads are simultaneously rearranged in the single queue.

Zolnowsky teaches using several queues to schedule operations. In particular, each one of the processors has a dedicated queue and a global dispatch (real time) queue is used for higher priority real time threads, as described in column 6, lines 27-33. As clearly shown in Figure 4A, a different dispatch queue is associated with each processor. In column 8, lines 19-30 *Zolnowsky* describes that each processor services threads from the real time queue and its own dedicated queue. Therefore, the thread processing order is not scheduled in any single queue. Nowhere does *Zolnowsky* teach

or suggest ordering the threads for all of the processors in a single queue. The Examiner relies on *Jones* for teaching of ordering threads based on latency information. A review of *Jones* shows that this reference also does not teach or suggest ordering the threads for all of the processors in a single queue.

Furthermore, *Zolnowsky* does not teach or suggest the limitation recited in amended claims 1 and 9 of simultaneously rearranging the order in which all threads will be serviced from the single queue. *Jones* also fails to teach or suggest simultaneously rearranging the order in which all threads will be serviced from the single queue.

Claims 1-15, 17-18, and 20

Claims 1-15, 17-18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Ramakrishnan* (U.S. Patent No. 6,085,215) and *Jones*. These rejections are respectfully traversed.

Ramakrishnan teaches using a round-robin scheduler to select each thread for execution from a real time domain and a general purpose domain. Nowhere does *Ramakrishnan* teach or suggest ordering the threads for all of the processors in a single queue and simultaneously rearranging the order in which all threads will be serviced from the single queue. *Jones* also fails to teach or suggest ordering the threads for all of the processors in a single queue and simultaneously rearranging the order in which all threads will be serviced from the single queue. The other references cited by the Examiner fail to cure the deficiencies of *Zolnowsky* and *Jones* relative to amended claims 1 and 9. Therefore no combination of the cited references can render either amended claim 1 or amended claim 9 obvious. For these reasons, Applicant submits that amended claims 1 and 9 are in condition for allowance and respectfully request withdrawal of the 35 U.S.C. § 103(a) rejection of these claims. Since claims 2-8, 17-18, and 21-22 depend from allowable claim 1 and claims 10-15 depend from allowable claim 9, these claims also are in condition for allowance.

New Claim 23

New claim 23 recites the limitation of the thread and at least one of the other threads corresponding to interrupt requests from a single one of the hardware devices,

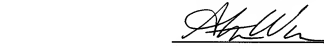
as described in paragraph [0032] of the present invention. Since new claims 23 depends from allowable claim 1 this claim is also in condition for allowance.

Conclusion

In conclusion, the references cited by the Examiner, alone or in combination, do not teach, show, or suggest the invention as claimed.

Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed. Applicants reserve the right to subsequently take up prosecution of the claims as originally filed in this application in a continuation, a continuation-in-part and/or a divisional application. If the Examiner has any questions, please contact the Applicants' undersigned representative at the number provided below.

Respectfully submitted,



Stephanie Winner
Registration No. 52,371
PATTERSON & SHERIDAN, L.L.P.
3040 Post Oak Blvd. Suite 1500
Houston, TX 77056
Telephone: (650) 330-2310
Facsimile: (650) 330-2314
Agent for Applicant